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Title: DELAY LOCKED LOP FOR AN FPGA ARCHITECTURE

Attorney: Kenneth D'Alessandro Sierra Patent Group, Ltd.

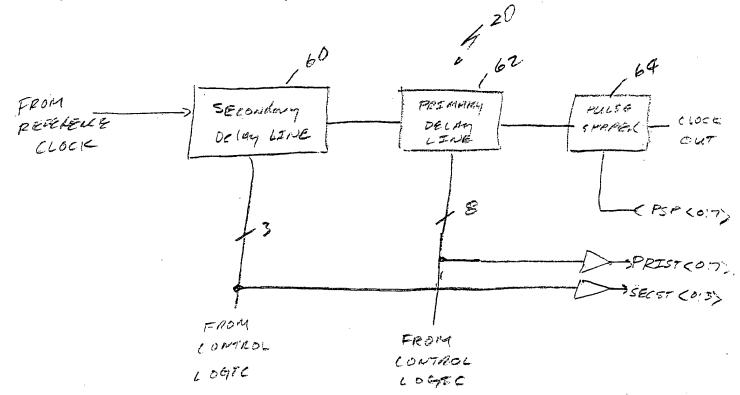


FIG. 2

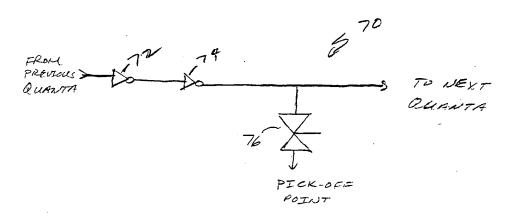
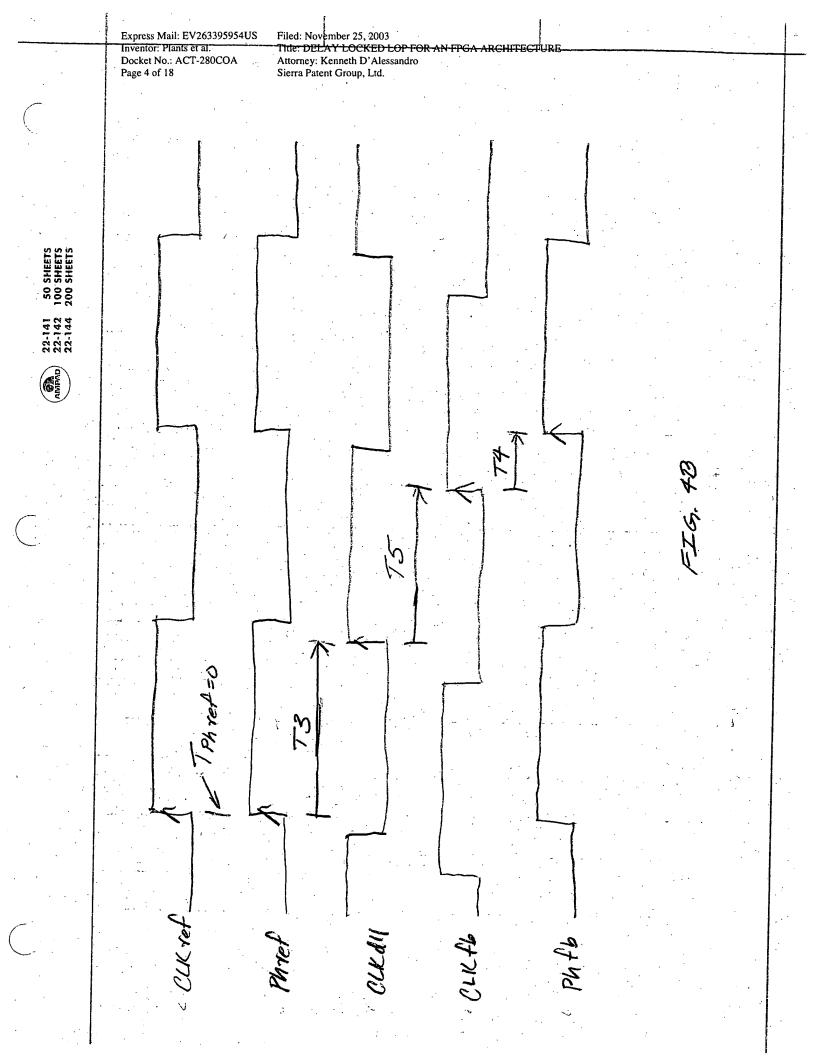


FIG. 3



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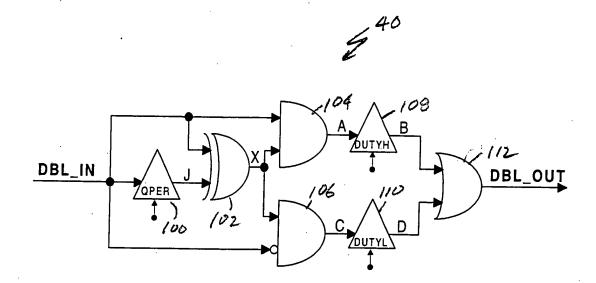


FIG. 5

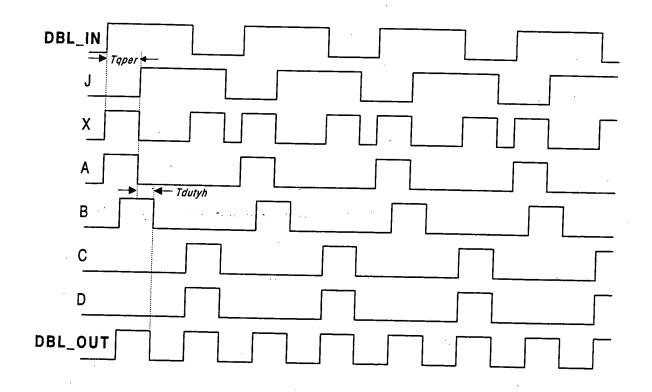


FIG. 6

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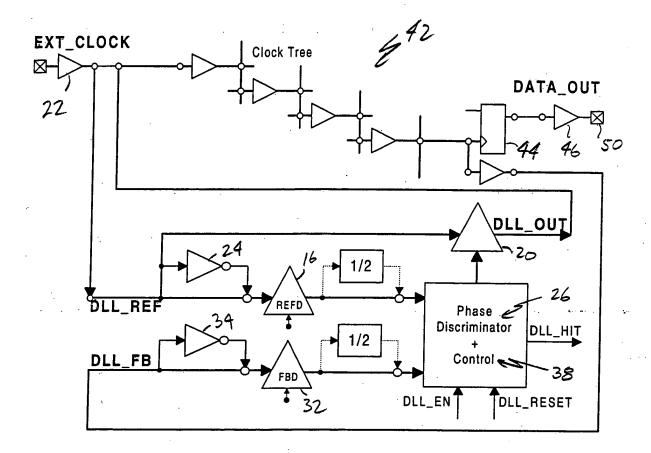


FIG. 7A

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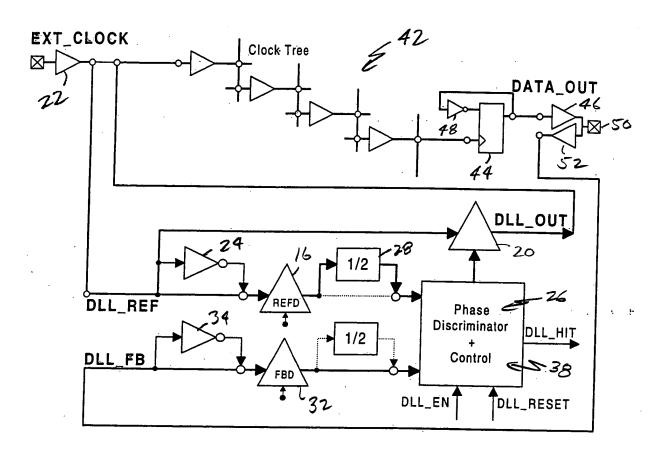


FIG. 73

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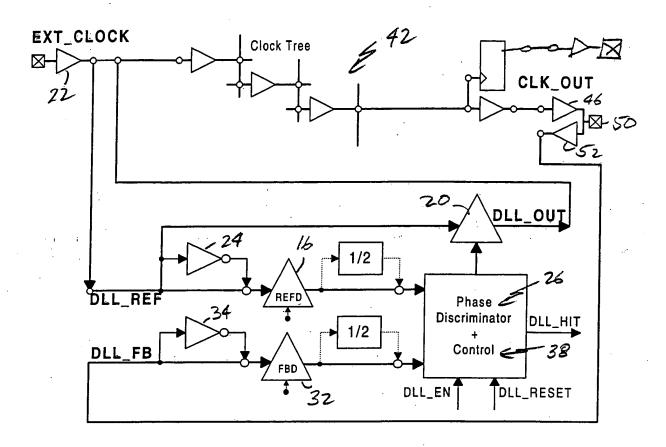
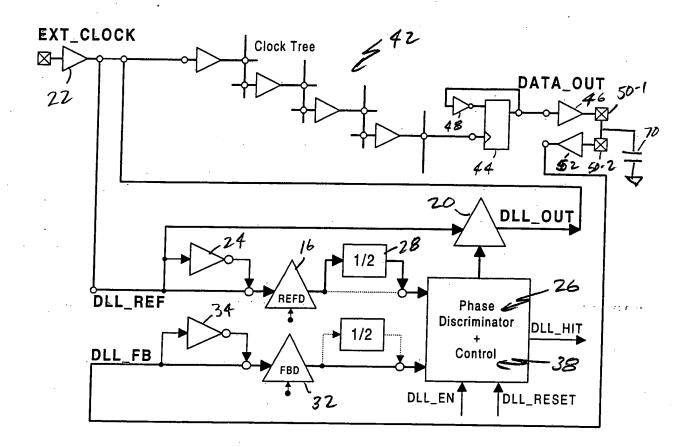


FIG. 7C

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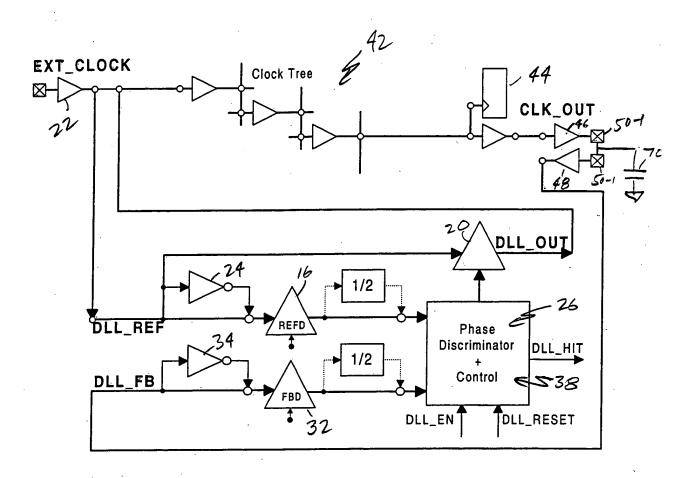


FIG. TE

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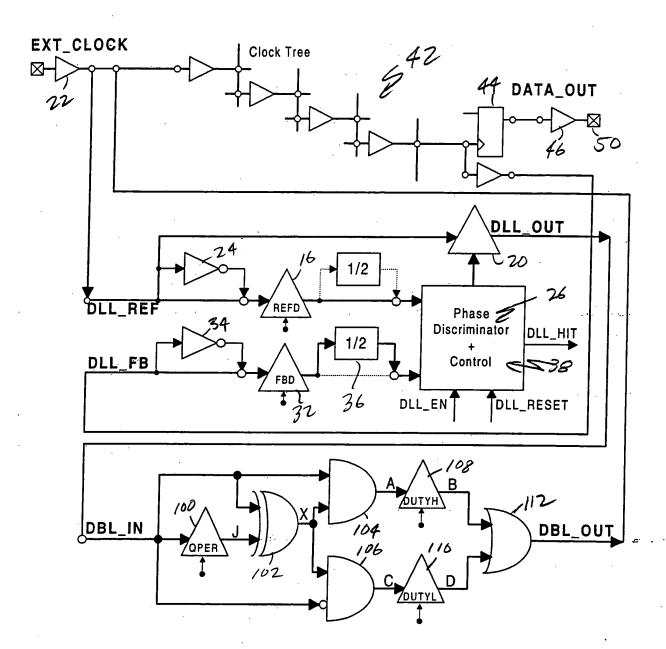


FIG. 7F

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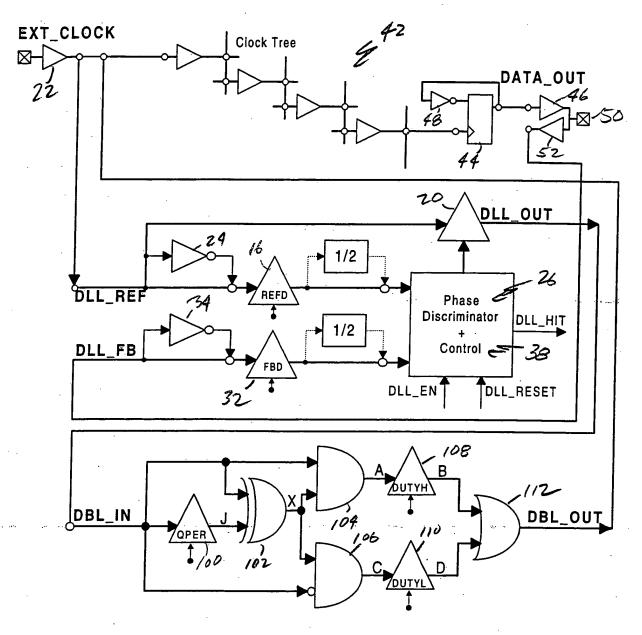


FIG. 79

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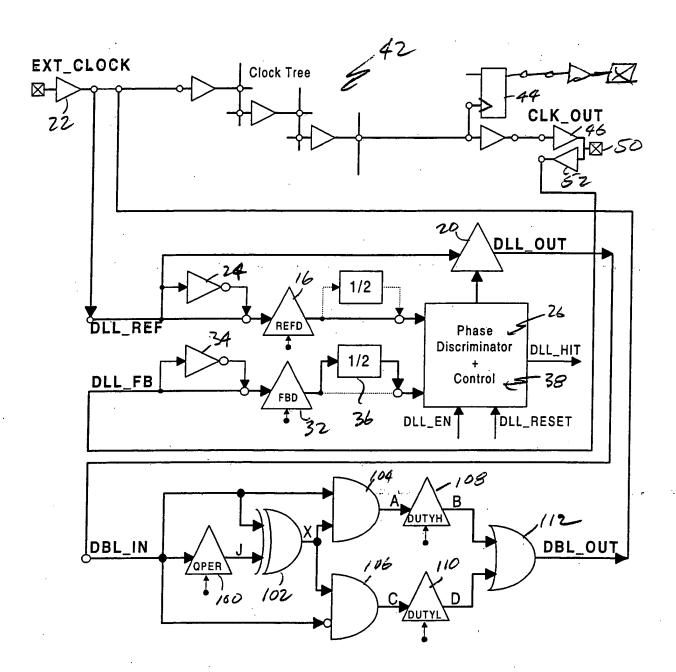


FIG. 7 H

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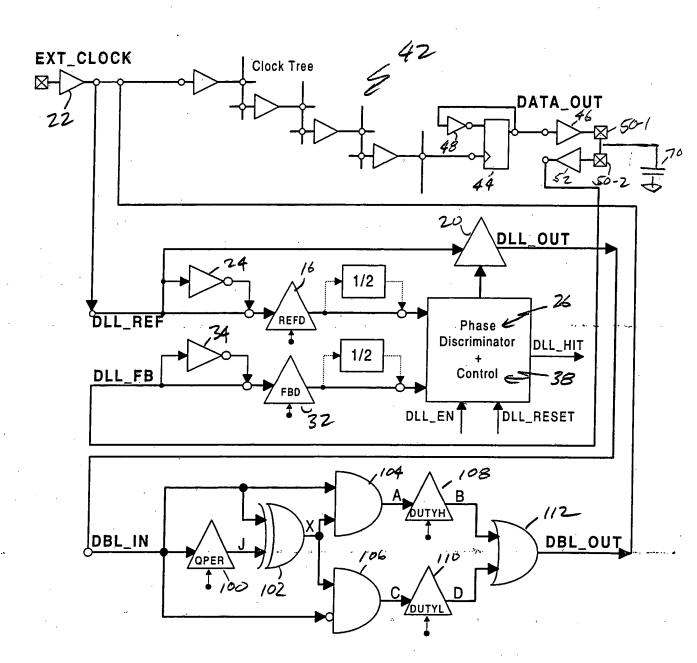


FIG. 7I

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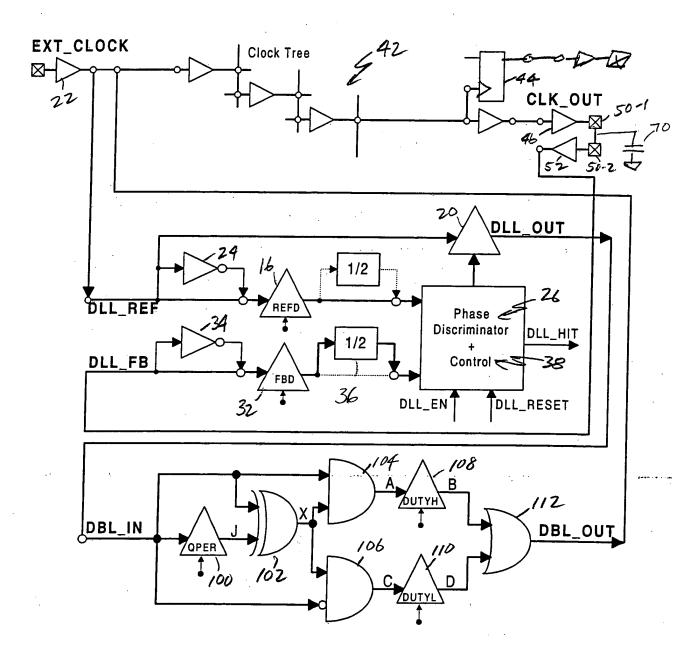


FIG. 7J

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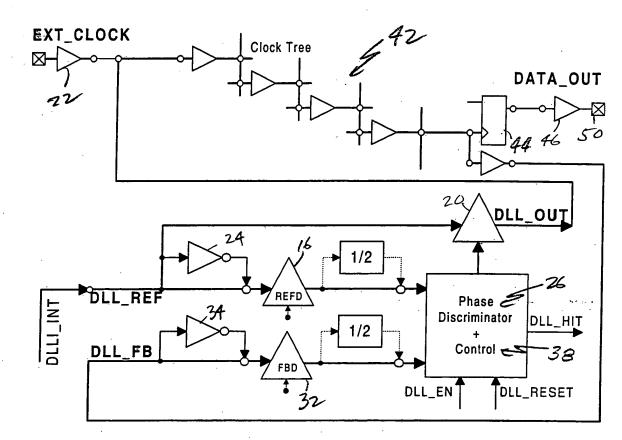


FIG. TK

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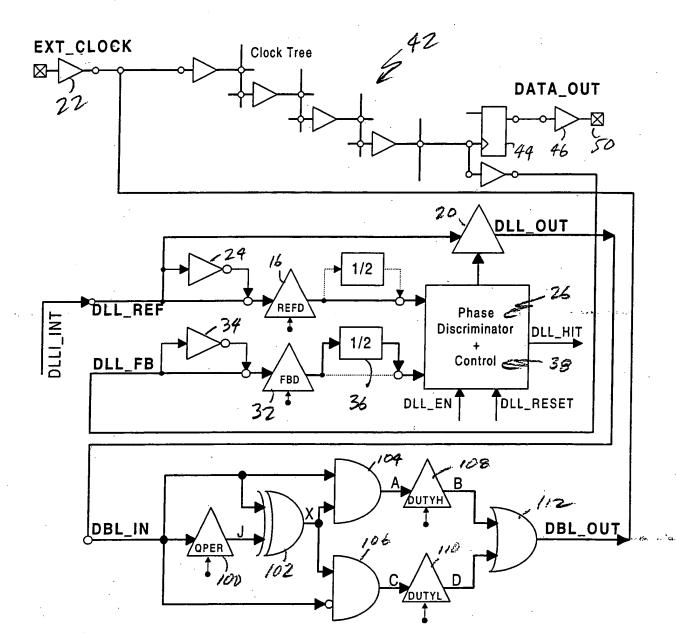


FIG. 7L